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APPLICATION

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ON

A METHOD AND APPARATUS FOR MEASURING THE COMMON-MODE COMPONENT OF A DIFFERENTIAL SIGNAL

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A METHOD AND APPARATUS FOR MEASURING THE COMMON-MODE COMPONENT OF A DIFFERENTIAL SIGNAL

BACKGROUND OF THE INVENTION

[0001] Field of the Invention

[0002] This invention relates to electronic systems and, more particularly, to common-mode detectors.

[0003] Description of the Related Art

[0004] Automatic test equipment (ATE) is used to test electric circuits prior to completing their manufacture. Although differential component detectors are relatively common in ATE, the use of common-mode detectors is relatively new. One such common-mode detector is described by C. Bishop in U.S. patent number 6,281,699. A window comparator generates an output indicative of whether the common-mode signal is above, within, or below predetermined thresholds to determine a common-mode component. Two buffers and a resistor pair are provided with the window comparator to extract the common-mode signal and reduce loading effects on input signals from a device under test (DUT).

[0005] Unfortunately, a substantial current can flow through the resistor pair when the comparator's input signals are separated by a large differential voltage. Thus, the buffers should be designed to source and sink the maximum expected current that can flow. Additionally,

the resistors must be made low in value in order to operate the circuit with high bandwidth. This adds to the problem of excessive current flow and can also cause significant nonlinearity in the response of the buffers.

[0006] There still exists a need, therefore, for a common-mode detector that does not suffer from large currents resulting from large input differential voltages and which does not suffer from high output impedance that precludes high bandwidth operation.

SUMMARY OF THE INVENTION

[0007] A common-mode detector is disclosed for determining the common-mode component of a differential signal. It includes a first difference amplifier that is connected to compare a first input voltage, preferably a noninverted component of the differential signal, with a feedback voltage to provide a first result. A second difference amplifier is connected to compare a second input voltage, preferably an inverted component of the differential signal, with the feedback voltage to provide a second result. A feedback amplifier is connected to drive the feedback voltage to a level that is substantially the average of the first and second input voltages in response to receiving the first and second results.

[0008] In one embodiment, a method is described for detecting the common-mode component. A voltage difference between the noninverted component of the differential signal and a feedback signal is converted to a first differential current signal. A voltage difference between the inverted component of the differential signal and the feedback signal is converted to a second differential current signal. The first and second differential current

signals are compared to generate the feedback signal, which settles to a voltage indicative of the common-mode component of the differential signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principals of the invention. Moreover, in the figures, like reference numerals designate corresponding parts throughout the different views.

[0010] Figure 1 is a block diagram of one embodiment of the invention with two differential amplifiers coupled to differential inputs V_A and V_B, respectively, with their outputs coupled to an op-amp for feedback.

[0011] Figure 2 is a schematic illustrating one implementation of the circuit illustrated in Figure 1, which has two transistor pairs for implementing the differential amplifiers.

[0012] Figure 3 is a flow diagram of an embodiment that compares input signals V_A and V_B to an output voltage V_O.

DETAILED DESCRIPTION OF THE INVENTION

[0013] A common-mode detector, in one embodiment, has two difference amplifiers for comparing each component of a differential signal to a feedback voltage. Each difference amplifier outputs a differential result that varies with the voltage difference between its respective differential signal component and the feedback signal. A feedback amplifier compares first and second results to generate the feedback voltage that is indicative of the difference between the first and second voltages. The

feedback voltage is driven by the feedback amplifier to a voltage representing the common-mode component of the differential signal.

[0014] Figure 1 illustrates a common-mode detector 100 that has, in one embodiment, two differential transconductance amplifiers and a feedback amplifier, preferably an operational amplifier (OA1), to generate a voltage proportional to the common-mode component of a differential signal. The noninverting and inverting components of the differential signal are received at input terminals V_A and V_B, respectively, of the detector 100. A first input V_{P1} of a differential transconductance amplifier gm1 is coupled to terminal V_A to receive the noninverting component of the differential signal. A second input V_{N1} of gm1 is coupled to the detector's output at terminal V_O for feedback. A second differential transconductance amplifier gm2 has first and second inputs V_{P2} and V_{N2}, with V_{P2} coupled to terminal V_B to receive the inverting component of the differential signal, and V_{N2} coupled to terminal V_O to receive feedback from the output of the detector 100. Consequently, both the gm1 and gm2 amplifiers receive feedback from terminal V_O at one of their two input terminals, and each is provided with a respective input of the differential signal at respective input terminals V_A and V_B. More particularly, gm1 is provided with the difference in voltage between terminals V_A and V_O, while gm2 is provided with the difference in voltage between terminals VB and V_O to form difference amplifiers.

[0015] On their output sides, gm1 and gm2 are coupled at their first outputs I_{P1} and I_{P2}, respectively, to a high impedance inverting input of an op-amp OA1 and to a DC reference voltage, Vcc, through a load impedance R1. Cur-

rent flows from I_{P1} and I_{P2} through R1 with the output currents from I_{P1} and I_{P2} each preferably equal to one-half of a bias current I_O plus a current proportional to the difference in input voltages between the inputs of the associated amplifiers gm1 and gm2. More particularly, the current from I_{P1} varies with the voltage difference between one side of the differential signal at terminal V_A and the feedback signal from terminal V_O. The current from I_{P2} varies with the voltage difference between the other side of the differential signal at terminal V_B and the feedback signal from terminal V_O. The resulting voltage at the inverting input is indicative of the voltages between terminals V_A/V_O and between V_B/V_O, respectively.

[0016] Second outputs I_{N1} and I_{N2} of gm1 and gm2, respectively, are coupled to a high impedance noninverting input of OA1. Both I_{N1} and I_{N2} are also coupled to a DC reference voltage (V_{CC}) through a second load impedance R2. Similar to I_{P1} and I_{P2}, their output currents flow through R2 and the current for each of I_{N1} and I_{N2} varies with the difference in the input voltages on the input sides of gm1 and gm2, respectively. However, the resulting output currents for I_{N1} and I_{N2} are preferably equal to half the base line bias output current I_O minus (rather than plus) a current proportional to the difference in voltages between the inputs of the associated amplifiers gm1 and gm2. The voltage at I_{N1} and I_{N2} is presented to the noninverting input for comparison to the voltage at the inverting input. Each of the outputs of gm1 and gm2 (I_{P1}, I_{N1} and I_{N2}, I_{P2}, respectively) are characterized by equations (1) and (2),

$$I_P = I_O/2 + \alpha(V_P - V_N) \qquad (1)$$

$$I_N = I_O/2 - \alpha(V_P - V_N) \qquad (2)$$

where α is a gain coefficient associated with the gm1 and gm2 amplifiers. α is either a fixed gain coefficient or a variable coefficient that, for a differential transconductance amplifier implemented with an ideal bipolar differential pair, is characterized by equation (3),

$$\alpha = [(I_O/Vt) * \exp(-Vd/Vt)] / [1+\exp(-Vd/Vt)]^2 \quad (3)$$

where Vt is the thermal voltage (kT/q), k is the boltzmann constant, q is electron charge, T is temperature in Kelvin, and Vd is equal to Vp-Vn. The output voltage at terminal V_O settles at a voltage between the differential input voltages at terminals V_A and V_B in response to receiving the results of the voltage comparison between V_A and V_B with V_O.

[0017] Figure 2 is an implementation of the embodiment illustrated in Figure 1, which has two NPN differential pair transistors Q1/Q2 and Q3/Q4 to implement gm1 and gm2, respectively. The differential pairs Q1/Q2 and Q3/Q4 are coupled to terminals V_A and V_B, respectively, at bases of Q1 and Q4, respectively, so that each differential pair receives one component of the differential signal. Bases of Q2 and Q3 are both coupled to the output of oA1 so that each differential pair receives one component of the differential signal for comparison against feedback from oA1. In the first differential pair Q1/Q2, emitters for Q1 and Q2 are coupled to a low voltage supply bus V_{EE} through a current source I_1. Similarly, emitters for Q3 and Q4 in the second differential pair are coupled to V_{EE} through a current source I2. Emitter degeneration resistors RE can also be provided between the low voltage supply bus V_{EE} and each of the emitters for Q1, Q2, Q3 and Q4 to reduce the gain and improve the linearity of the differential pairs Q1/Q2 and Q3/Q4.

[0018] Output collectors for Q2 and Q3 are coupled to V_{CC} through impedance R2 so that the voltage at the noninverting input of OA1 is determined by the value of the R2 resistor multiplied by the sum of Q2 and Q3 currents. Similarly, the output collectors for Q1 and Q4 are coupled to a positive DC reference voltage through impedance R1 so that the voltage at the inverting input of OA1 is determined by the value of resistor R1 multiplied by the sum of the Q1 and Q4 currents. Preferably, the impedances R1 and R2 are equal, so that the voltages at the inverted and noninverted inputs of OA1 are the same when the sum of the Q2 and Q3 currents matches the sum of the Q1 and Q4 currents.

[0019] The current sources I_1 and I_2 are preferably matched so that an equal voltage differential between the bases of Q1/Q2 and those of Q3/Q4 produces voltages at the inverting and non-inverting inputs of oA1 that are substantially equal to one another. The equal voltage differentials are accomplished by oA1 driving its output at terminal V_O to a voltage centered approximately between the inputs of V_A and V_B. Such a voltage is approximate to the average or common-mode voltage V_{CM} so that the output at terminal V_O settles at a voltage indicative of the common-mode component of the differential signals.

[0020] For a common-mode detector designed for a differential voltage across V_A and V_B of between -1.0V and 1.0V, and a common-mode voltage V_{CM} between -1.0V and +1.0V, the components could the following values:

R1, R2 = 1Kohm
R_E = 100ohm
I_1, I_2 = 1mA

[0021] Although the differential transconductance amplifiers are illustrated using NPN bipolar transistors, they could instead be implemented using any transconductance device, including (but not limited to) bipolar, metal oxide semiconductor (MOS) or junction field effect transistors (JFET).

[0022] Figure 3 is a logical flow diagram illustrating a method of detecting a common-mode component in a differential signal for a common-mode detector. The method begins with differential components V_A and V_B provided to the detector and with an output V_O from the detector (block 300). The voltage of output V_O is subtracted from the voltage of each differential component V_A and V_B to produce respective currents ΔiA and ΔiB (blocks 305, 310) that are indicative of the voltage difference at the respective inputs to each gm amplifier. More particularly, the voltage subtraction between V_A and V_o results in a current Δi_A indicative of the difference in voltages for use by the detector. Similarly, the voltage comparison between V_B and V_O results in a current Δi_B. If Δi_A is substantially equal to Δi_B (block 315) then V_O remains unchanged and the cycle starts back at the beginning (block 300). If Δi_A is greater than Δi_B (block 320) then the voltage level for output V_O is moved closer to the voltage level for V_A (block 325). In the embodiment illustrated in Figure 2, a Δi_A larger than Δi_B would produce a larger voltage drop across R1 than across R2. The inverting input of the feedback amplifier would be presented with a smaller voltage than would the noninverting input, and thus the V_O feedback signal would be driven toward V_A. If instead, Δi_A is less than Δi_B (block 320) then the voltage level for output V_O is moved closer to the voltage level

for V_B (block 330). The process repeats with differential signals V_A and V_B and newly modified output V_O (block 300). In this manner, the detector uses its own voltage output V_O as feedback for comparison to the differential components V_A and V_B.

[0023] Or, the common-mode detector can generate voltages Δv_A and Δv_B, instead of currents Δi_A and Δi_B, in response to comparing the voltages of V_A and V_B with the output voltage V_O. The voltages ΔvA and Δv_B would be indicative of the difference in voltage between V_A and V_O, and V_B and V_O, respectively. V_O would settle at a voltage level approximating the average of V_A and V_B, which defines the common-mode voltage V_{CM}.

[0024] While various embodiments of the invention have been described in terms of a common-mode detector in an ATE, it will be apparent to those of ordinary skill in the art that many more embodiments and implementation are possible within the scope of this invention that are removed from an ATE, such as in other circuits requiring detection of the common-mode, or average, component of a differential signal. Accordingly, the invention should be limited only in terms of the appended claims.